## REMARKS:

Claims 5-7, 16 and 17 are pending in the application. By this amendment, claims 16 and 17 are being amended to improve their form. No new matter is involved.

Upon filing the CPA application on April 5, 2001, applicant requested and paid the fee for a 3 month suspension of action. Nevertheless, the Office Action of June 22, 2001 was issued before the 3 month period following the filing of the CPA terminated. In a telephone conversation between the undersigned and Examiner Tran on August 9, 2001 to discuss this, it was agreed that the Office Action of June 22, 2001 would stand and, if applicant files a prompt response thereto, the next Office Action will not be made final.

Claim 16 is being amended to add various limitations of claim 17 thereto, and in view thereof, claim 17 is being rewritten in independent form. Additionally, claim 17 is amended to overcome the formal rejection set forth in the Office Action as described hereafter.

In paragraph 1 on page 2 of the Office Action, claim 17 is objected to because the recitation in line 13 of "said element separate regions" should read -- said element separating regions. Claim 17 is being amended to make this change.

Also, in paragraph 3 which begins on page 2 of the Office Action, claim 17 is rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter not described in the specification. Specific objections are then set forth in the

paragraph. In response thereto, applicant is amending the paragraph which previously read "each of said floating gates is not formed on said element separating regions, but is formed only on each of said memory transistors in said memory regions" to read -- each of said floating gates is formed on each of said memory transistors between and to the exclusion of most of said element separating regions". Similarly, the last paragraph of the claim is being amended so as to recite that in each of the element separating regions, both the oxide film and the another oxide film are formed between each sidewall and each of the control gates, thereby eliminating the reference to floating gates therefrom. As so amended, claim 17 now corresponds with the embodiments shown and described in the specification.

In paragraph 5 on page 3 of the Office Action, claim 17 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite, and in the following paragraph 6, the limitation "said memory regions which appears in lines 10, 12 and 14 is said to have insufficient antecedent basis. In response thereto, the objected-to phrases are being changed to refer to the memory transistors.

Consequently, claim 17 as amended herein should now be clear and definite. Such claim is clearly supported by the specification. Moreover, claim 17 was not rejected on prior art and the Office Action. Therefore, inasmuch as the informalities of the claim have been remedied, such claim should now be in condition for allowance.

In paragraph 8 which begins on page 3 of the Office Action, claims 5, 6 and 16 are rejected under 35 U.S.C. § 103(a), as being unpatentable over U.S. Patent

5,068,697 of Noda et al. in view of reference U or U.S. Patent 5,434,093 of Chau et al. or U.S. Patent 5,518,945 of Bracchitta et al. Noda et al. is said to disclose the claimed subject matter except for certain features, such as sidewalls 26 formed of LPCVD silicone nitride. Moreover, phosphorus silicate glass (PSG) and LPCVD silicone nitride are dielectric materials known in the art and routinely used to form protective sidewall spacers in semiconductor devices, as shown for example by reference U, Bracchitta et al. and Chau et al. Chau et al. is said to disclose other materials suitable for constructing spacers, including nitride, BSG and PSG. Bracchitta et al. is said to disclose LPCVD nitride being used as spacers. Reference U is also said to disclose LPCVD nitride used as spacers. These rejections are respectfully traversed, particularly in view of claim 16 as amended herein.

As applicant has previously pointed out, the present invention relates to a floating gate memory where the individual transistors have a floating gate having a structure that limits damage to the tunnel oxide from the manufacturing process. In particular, the floating gate transistor preferably includes an oxide layer alongside the floating gate and control gates, sidewall spacers formed from LPCVD silicone nitride on the oxide layer, and a capping nitride layer. The LPCVD silicone nitride spacers can be formed in a manner that does not degrade the tunnel oxide. The LPCVD silicone nitride spacers protect the gate oxide from subsequent processing steps using plasma processors that might introduce hydrogen to the tunnel oxide.

While the various newly applied references such as Reference U, Bracchita et al. and Chau et al. are cited for their alleged showing of the obviousness of various materials disclosed therein, the attempted combination of Noda et al. therewith does not overcome the basic deficiencies of such combinations when compared with structures according to the invention. Thus, in claim 16 as amended, various limitations of claim 17 are added to the basic combination of the nonvolatile semiconductor memory device, which device includes a semiconductor substrate, memory transistors, an oxide film, side walls, a second silicone nitride film, and a wiring layer. As amended, the combination of claim 16 further includes the various features in accordance with the invention including element separating regions extending along one direction, groups of the memory transistors being arranged along the one direction and adjacent the element separating regions, and element separating insulating film in each of the element separating regions, formed on the substrate extending in the one direction, each of the floating gates being formed on each of the memory transistors between and to the exclusion of most of the element separating regions, and the control gates extending in a direction perpendicular to the one direction and intersecting the memory transistors and the element separating regions, and each of the control gates being arranged on the element-separating insulating films in the element separating regions. The prior art does not disclose or suggest such combination in accordance with the invention. Therefore, claim 16 as amended is submitted to clearly distinguish patentably over the prior art. Claims 5-7 depend, directly or indirectly, from claim

16, and contain all of the limitations thereof so as to also distinguish patentably over the prior art.

In conclusion, claims 5-7, 16 and 17 are submitted to clearly distinguish patentably over the prior art for the reasons discussed above. Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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**Version with markings to show changes made:**

Rewrite claim 16 as follows:

16. (Amended) A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

memory transistors formed on said semiconductor substrate to perform nonvolatile storage of an electric charge in accordance with data, each of said memory transistors being an electrically rewritable memory transistor including a floating gate formed over said semiconductor substrate via a first gate insulating film and a control gate formed over said floating gate via a second gate insulating film;

an oxide film formed on said substrate and at least on both sides of each said floating gate and both sides of each said control gate;

side walls each for protecting sides of said floating gate and said control gate of each said transistor, each said side wall formed from a first silicon nitride film formed by low-pressure CVD over said oxide film;

a second silicon nitride film covering surfaces of said control gate, a source diffusion layer, a drain diffusion layer and each of said side walls of each of said memory transistors and on surfaces; [and]

a wiring layer formed over said second silicon nitride film via an inter-layer insulating film[.]; and

element separating regions extending along one direction; and wherein

groups of said memory transistors are arranged along said one direction and adjacent said element separating regions;

in each of said element separating regions, an element separating insulating film is formed on said substrate extending in said one direction;

each of said floating gates is formed on each of said memory transistors between and to the exclusion of most of said element separating regions; and

said control gates extending in a direction perpendicular to said one direction and intersecting said memory transistors and said element separating regions, each said control gate being arranged on said element-separating insulating films in said element separating regions.

Rewrite claim 17 as follows:

17. (Twice Amended) [The nonvolatile semiconductor memory device according to claim 16, further comprising:]

A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

memory transistors formed on said semiconductor substrate to perform nonvolatile storage of an electric charge in accordance with data, each of said memory transistors being an electrically rewritable memory transistor including a floating gate formed over said semiconductor substrate via a first gate insulating film and a control gate formed over said floating gate via a second gate insulating film;

an oxide film formed on said substrate and at least on both sides of each said floating gate and both sides of each said control gate;

side walls each for protecting sides of said floating gate and said control gate of each said transistor, each said side wall formed from a first silicon nitride film formed by low-pressure CVD over said oxide film;

a second silicon nitride film covering surfaces of said control gate, a source diffusion layer, a drain diffusion layer and each of said side walls of each of said memory transistors and on surfaces;

a wiring layer formed over said second silicon nitride film via an inter-layer insulating film; and

element separating regions extending along one direction, wherein

groups of said memory transistors are arranged along said one direction and adjacent said element separating regions;

in each of said element separating regions, an element separating insulating film is formed on said substrate extending in said one direction;

each of said floating gates is [not formed on said element separating regions, but is] formed [only] on each of said memory transistors [in said memory regions] between and to the exclusion of most of said element separating regions;

said control gates extending in a direction perpendicular to said one direction and intersecting said memory [regions] transistors and said element separating regions, each said control gate being arranged on said element-separating insulating films in said element [separate] separating regions;

in each of said memory [region] transistor, both said oxide film and another oxide film are formed between each said side wall and each said floating and control gates, and are formed between each said side wall and said substrate; and

in each said element separating region, both said oxide film and said another oxide film are formed between each said side wall and each said [floating and] control gates, and only said another oxide film is formed between each said side wall and each element separating insulating film.